

Amendments to the Claims

1. (*Currently Amended*) An integrated protection circuit for an integrated circuit device, comprising:
[[-]] a first transistor (~~MP1~~) whose control outputs are connected between a pad (~~2,3~~) and a control input of a clamping device (~~MN4~~),
[[-]] control outputs of said clamping device (~~MN4~~) being connected between said pad (~~2,3~~) and a reference voltage terminal (4),
[[-]] a second transistor (~~MN3~~) whose control outputs are connected between the control output of said first transistor (~~MP1~~) and said reference voltage terminal (4), and
[[-]] time-delay means (~~R, MN1~~) connected between a supply voltage terminal (1) and said control inputs of said first transistor (~~MP1~~) and said second transistor (~~MN3~~).
2. (*Currently Amended*) The protection circuit according to claim 1, wherein the pad (~~2,3~~) is a signal pad (2) or a power supply pad (3).
3. (*Currently Amended*) The protection circuit according to claim 1 or 2, according to claim 1, wherein the time-delay element (~~R, MN1~~) comprises a series connection of a resistor (~~R~~) and a capacitance.
4. (*Currently Amended*) The protection circuit according to claim 3, wherein the time-delay element (~~R, MN1~~) comprises a third transistor (~~MN1~~), the resistor (~~R~~) being connected between the supply voltage terminal (1) and said third transistor (~~MN1~~), said third transistor (~~MN1~~) forming the capacitance.
5. (*Currently Amended*) The protection circuit according to claim 4, wherein a fourth transistor (~~MN2~~) is provided whose control outputs are connected between the reference voltage terminal (4) and the control output of the third transistor (~~MN1~~) and whose control input is connected to said reference voltage terminal (4).

6. (*Currently Amended*) The protection circuit according to claim 1, ~~any preceding claim~~, wherein the first transistor (MP1) is a p-channel MOS transistor.

7. (*Currently Amended*) The protection circuit according to claim 1, ~~any preceding claim~~, wherein the second, third and fourth transistor (~~MN1, MN2, MN3~~) are n-channel MOS transistors.

8. (*Currently Amended*) The protection circuit according to claim 1, ~~any preceding claim~~, wherein the clamping device (~~MN4~~) is a n-channel MOS transistor ~~layouted for ESD~~ laid out for ESD protection.

9. (*Currently Amended*) The protection circuit according to claim 1, ~~any of the preceding claims 1 to 7~~, wherein the clamping device (~~MN4~~) is a parasitic npn transistor.

10. (*Currently Amended*) The protection circuit according to claim 1, ~~any of the preceding claims 1 to 7~~, wherein the clamping device (~~MN4~~) is a thyristor.

11. (*Currently Amended*) The protection circuit according to claim 1, ~~any preceding claim~~, wherein a diode (~~D~~) is connected between the pad (~~2~~) and the supply voltage terminal (~~1~~).